



# My Head Hurts, My Timing Stinks, and I Don't Love On-Chip Variation

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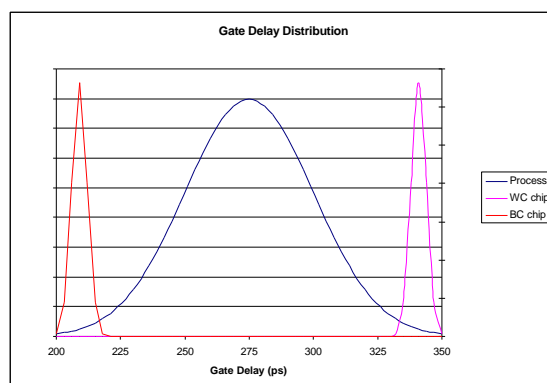
Insert Paper Title here

- On-chip Variation. What is it? Where does it come from?
- What problems can OCV cause?
- Example path before OCV analysis
- How to turn on OCV analysis
- Example path after OCV analysis
- CRPR
- Surprise
- Conclusions

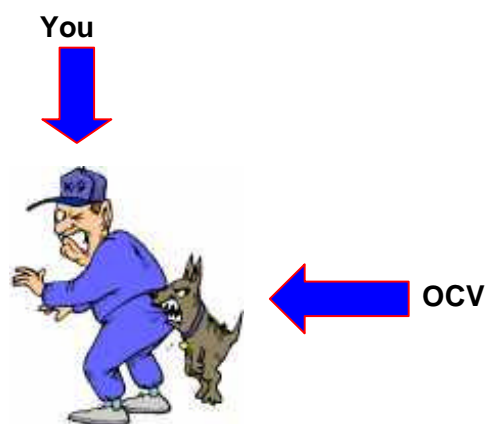


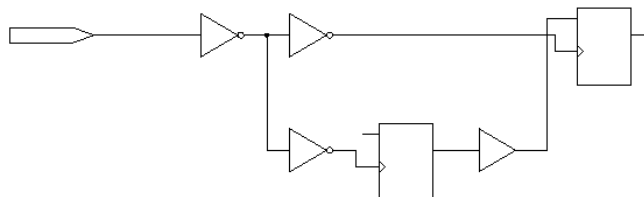
- Modeled differences between two gates
  - Drive strength
  - Capacitive load
  - Input transition time
- Un-modeled differences between two gates
  - IR drop
  - Local thermal deltas
  - Optical Proximity Correction (OPC) differences/errors
  - Manufacturing variations

- Is delay a single fixed number?
- Is delay a pair of fixed numbers (best/worst case)?
- Delay as a probability distribution function.
- Distribution for entire process
- Distribution for individual chip
- On worst case chip, not all gates have worst case delay
- On best case chip, not all gates have best case delay



Best case/Worst case analysis is not good enough!!





```
> Report_timing -nosplit -input_pins -delay min -to
    [get_pins $min_pin] -path_type full_clock
```

Path Type: min

Point	Incr	Path
-----		
clock clk (rise edge)	0.00	0.00
clock source latency	0.00	0.00
clk (in)	0.00	0.00 r
clk_box_2_1/A (CLKI_Q)	0.00	0.00 r
clk_box_2_1/Z (CLKI_Q)	0.24 +	0.24 f
clk_box_1_10/A (CLKI_O)	0.16 *	0.40 f
clk_box_1_10/Z (CLKI_O)	0.26 +	0.66 r
tx_py/o_tstat0/E (D_F_LPH0001_H)	0.06 *	0.72 r
tx_py/o_tstat0/L2 (D_F_LPH0001_H)	0.10	0.82 f
tx_ll/U371/A (BUFFER_F)	0.00	0.82 f
tx_ll/U371/Z (BUFFER_F)	0.06	0.88 f
tx_ll/tstat_reg_0/D (D_F_LPH0001_LPC_E)	0.00	0.88 f
data arrival time		0.88

clock clk (rise edge)	0.00	0.00
clock source latency	0.00	0.00
clk (in)	0.00	0.00 r
clk_box_2_1/A (CLKI_Q)	0.00	0.00 r
clk_box_2_1/Z (CLKI_Q)	0.24 +	0.24 f
clk_box_1_8/A (CLKI_O)	0.16 *	0.40 f
clk_box_1_8/Z (CLKI_O)	0.26 +	0.66 r
tx_ll/tstat_reg_0/E (D_F_LPH0001_LPC_E)	0.06 *	0.72 r
clock uncertainty	0.10	0.82
tx_ll/tstat_reg_0/E (D_F_LPH0001_LPC_E)		0.82 r
library hold time	-0.03	0.79
data required time		0.79
-----		
data required time		0.79
data arrival time		-0.88
-----		
slack (MET)	<b>Lots of positive slack</b>	0.09



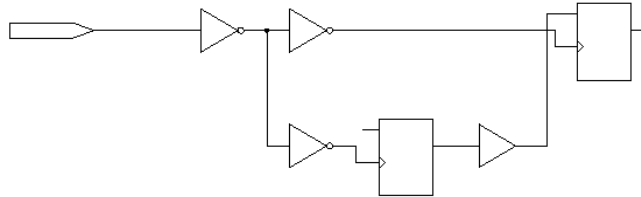
- Lots of positive slack: +90ps
- Clock arrival time is the same at the startpoint and endpoint registers

- Need to specify other side of single chip distribution
- Several methods to do this
  - Look in paper or Primetime User's Manual
- Use the method detailed in the app note from your ASIC vendor
- Method here uses simple scaling factors
  - > `set_operating_conditions -analysis_type`  
`on_chip_variation $BC_OP_CON`
  - > `set_timing_derate -min 1.0 -max 1.2`
- Typical variation 6-10%

**Max Clock Paths Derating Factor : 1.20**

Point	Incr	Path
-----		
clock clk (rise edge)	0.00	0.00
clock source latency	0.00	0.00
clk (in)	0.00	0.00 r
clk_box_2_1/A (CLKI_Q)	0.00	0.00 r
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data arrival time		0.88

clock clk (rise edge)	0.00	0.00	
clock source latency	0.00	0.00	
clk (in)	0.00	0.00	r
clk_box_2_1/A (CLKI_Q)	0.00	0.00	r
clk_box_2_1/Z (CLKI_Q)	<b>0.29</b>	+	<b>0.29</b> f
clk_box_1_8/A (CLKI_O)	<b>0.19</b>	*	<b>0.48</b> f
clk_box_1_8/Z (CLKI_O)	<b>0.31</b>	+	<b>0.79</b> r
tx_ll/tstat_reg_0/E (D_F_LPH0001_LPC_E)	<b>0.07</b>	*	<b>0.86</b> r
clock uncertainty	0.10		0.96
tx_ll/tstat_reg_0/E (D_F_LPH0001_LPC_E)			0.96 r
library hold time	-0.03		0.93
data required time			0.93
-----			
data required time			0.93
data arrival time			-0.88
-----			
slack (VIOLATED)			-0.05



- Clock Reconvergence Pessimism Removal
- A gate common to both the data and clock path can't be fast for one and slow for the other
- CRPR gives a credit for the difference between min and max delays along the common path
- `set timing_remove_clock_reconvergence_pessimism true`

Max Clock Paths Derating Factor : 1.20

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clk_box_2_1/Z (CLKI_Q)	0.29 +	0.29 f
clk_box_1_8/A (CLKI_O)	0.19 *	0.48 f
clk_box_1_8/Z (CLKI_O)	0.31 +	0.79 r
tx_ll/tstat_reg_0/E (D_F_LPH0001_LPC_E)	0.07 *	0.86 r
<b>clock reconvergence pessimism</b>	<b>-0.05</b>	<b>0.81</b>
clock uncertainty	0.10	0.91
tx_ll/tstat_reg_0/E (D_F_LPH0001_LPC_E)		0.91 r
library hold time	-0.03	0.88
data required time		0.88
-----		
data required time		0.88
data arrival time		-0.88
-----		
slack (MET)		0.00

- Turned off by default
- Noticeable increase in runtime and memory usage
  - `set timing_crpr_threshold_ps 20`
- Should opposite edges be given CRPR credit?
  - `set timing_clock_reconvergence_pessimism normal`
  - `set timing_clock_reconvergence_pessimism same_transition`



- Does OCV Analysis steal performance?
- Many ASIC vendors don't require OCV Analysis
- But, OCV still exists
- Other ways to handle OCV
  - Reduced yield
  - Pad setup and hold margins
  - Conservative library
  - Extra clock uncertainty
  - XX ps of positive slack for timing signoff
- These methods penalize all paths in design
- With OCV analysis plus CRPR, paths in common branch of clock tree can hold more logic

- Setup, hold, and clock gating examples
- Methods for specifying OCV
- Einstimer vs. Primetime comparison
- Tcl for constraints and DDR outputs.

- Looked at what OCV is
- Where it comes from
- How to model it
- Effect on Timing Reports
- CRPR
- How OCV/CRPR can actually improve performance