

**Cadence Analog Artist Mixed-signal Design  
and High Speed Simulation.**

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## Cadence Analog Artist Mixed-Signal Design and High Speed Simulation.

### Abstract

The paper will discuss a methodology we use at Fairchild to design mixed-signal devices. This process has been improved with the integration of a third party high speed simulator(HSIM). The ability to characterize digital subcells quickly and modify the synthesis design early in the design cycle has many advantages. The time required to run a full top-level spice simulation can be a major issue in the design process. Accelerated simulation provides a methodology to resolve many of these issues. We have also added the ability to batch to a Linux based system.

This allows simulation to run faster on less expensive systems. The spectreS simulation can run on the Unix based system in parallel. The paper will discuss our implementation and issues/limitations of the process in the Analog Artist Mixed-signal environment.

### Introduction

There are several methodologies for implementing a mixed-signal design. The top down design style and the bottom up cell design style need to be considered when selecting the applications and flow for design creation. The two mixed-signal flows provided by Cadence are the Cadence AMS simulator and the Analog Artist Mixed-signal Design Environment. The Cadence AMS Designer provides a single threaded simulation executable for simulation, supports spice/spectreS, Verilog AMS and SignalScan waveform viewer. The Analog Artist Environment is a mixed Spice and Verilog simulation environment. The connection

between the simulators is done with interface elements and interprocess communication. We were using the Analog Artist Mixed-signal design environment. The process of changing to Cadence AMS would require too many resources and would not be production ready in time. We decided to continue using Analog Artist Mixed-signal design environment.

At Fairchild Semiconductor, we were planning on updating our current mixed-signal design process. We were also reviewing high-speed simulators. A spectreS simulation of a large analog block or top level design could run for days and create very large psf files. Reading the files with the Analog Artist waveform viewer would take 20-30 minutes and would take 10 minutes to redraw. This made the software unusable.

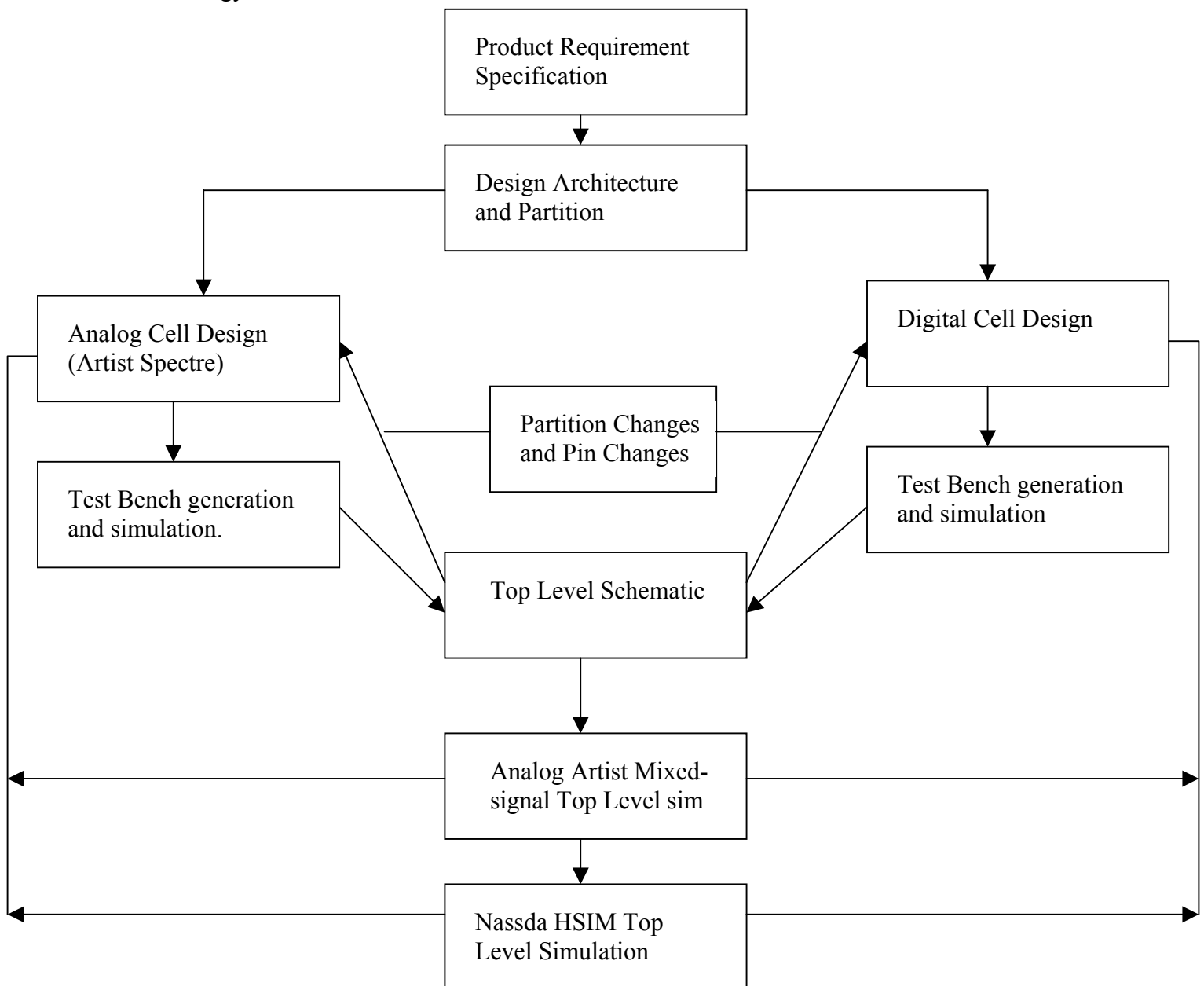
The first approach was to purchase faster hardware. The fact that SpectreS does not support Linux limited us to using fastest Sun systems. This was not fast enough and the waveform viewer was still too slow. We reviewed running Hspice on Linux. Even doubling the simulation speed, we still needed faster simulations and the waveform viewer continued to be an issue.

We reviewed the high speed simulators available from Nassda, Synopsis and other companies and decided to use Nassda HSIM. The HSIM simulator has many features we needed for Digital design. Power and timing simulation, in addition to high speed simulation, are examples of these features. The HSIM simulator supports an Analog Artist Simulation interface, Linux OS and a variety of waveform viewers. This paper will describe these features in more detail. In our first set of designs, we netlisted from Analog Artist and

used this netlist with HSIIM on a command line. A spectreS simulation ran for over 32 hours and we were able to run in less than 7 with HSIIM on a Sun workstation. The design group recognized the value of the simulator and requested the Analog Artist Interface for HSIIM be installed and added to the process libraries.

## New design Methodology

This is a top-level view of the combined Analog Artist Mixed-signal and Nassda HSIIM methodology.

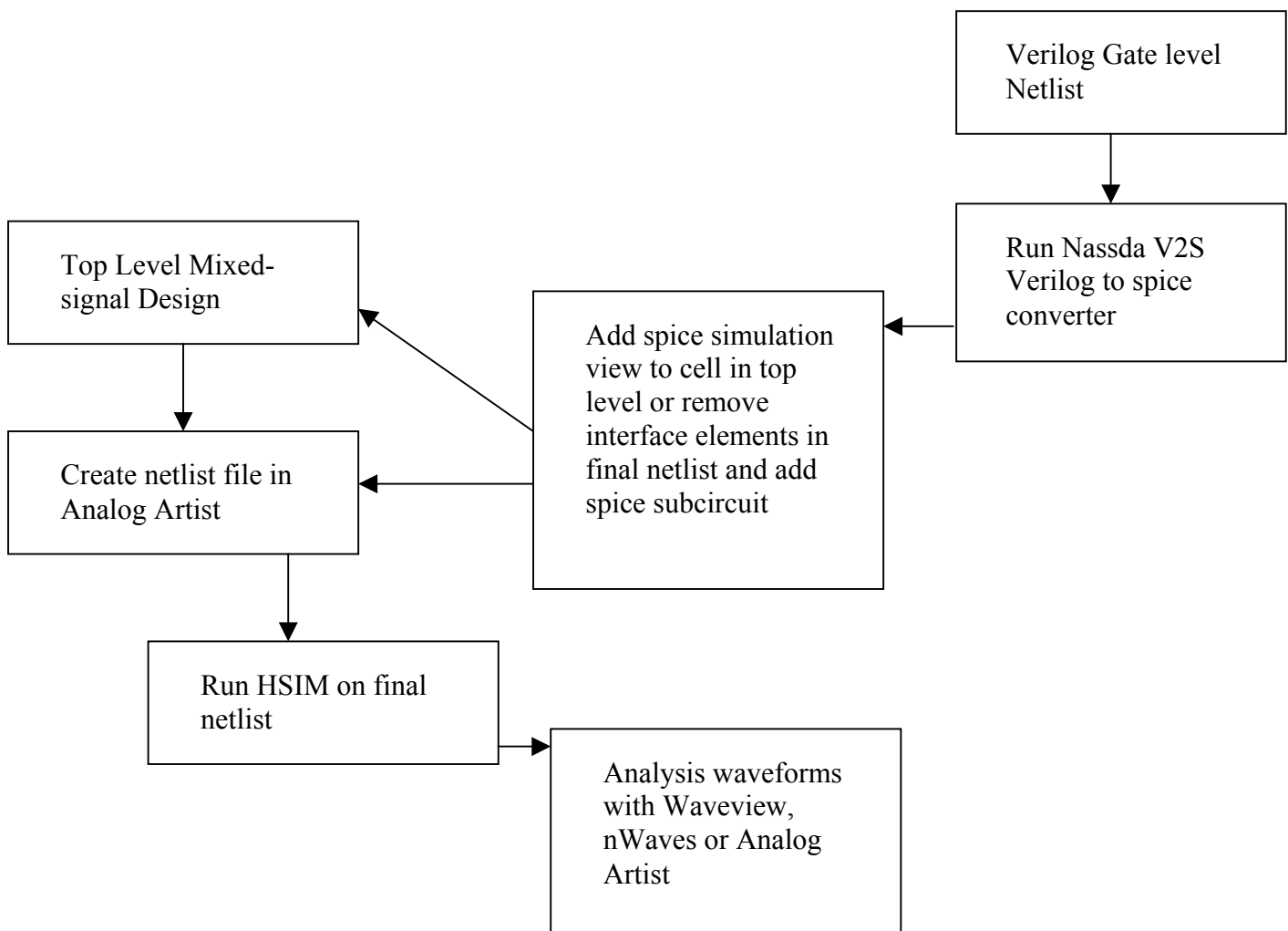


In this methodology HSIM is added to the existing Analog Artist mixed-signal design flow. This allows the designer to choose the simulation that is required for the design. Spice simulation for the accuracy needed in cell design, digital for the Verilog design, Analog Artist Mixed-signal for top level simulation and HSIM for more accurate than mixed-signal and faster than spice. With HSIM integrated in to the Analog Artist environment, it is also used in the larger Analog cell development or to simulate cells that require longer simulation time e.g. PLLs.

## Analog Mixed-signal Top Level Design Conversion

We are implementing two approaches to the conversion of the mixed-signal top level design. The first approach is to netlist the design and if needed modify the top level netlist. This requires no library updates and is easy to implement. The second is to create HSIM views and HSIM cdf sim info view for the libraries and integrate into our existing simulation environment. We currently use skill programs to set model paths, select different simulators (spectre, hspice), set simulation variables to select model types/speed and batch corner simulations. Nassda provides skill routines to assist in updates. We will be updating our production environment to support this in the near future. I will describe both processes.

### Top Level Netlist Methodology



The netlist approach requires the designer to manually update the netlist or add a spice subcircuit call to the Analog Artist cell symbol. The design is netlisted using spectreSverilog or spectreS. This process requires netlist file control. Modifying netlist and symbol view can cause errors if you are not careful. There are advantages to this process. If the analog portion of the design is stable and the digital netlist is changing you can update quickly and rerun simulations. We may improve this process by standardizing the cdf file updates for Analog Artist cells and perl scripts for updating netlist.

## **HSIM Analog Artist Methodology**

The HSIM User manual provides detailed information on updating Analog Artist libraries to support the HSIM simulator. I will go through an overview of the steps to convert a library.

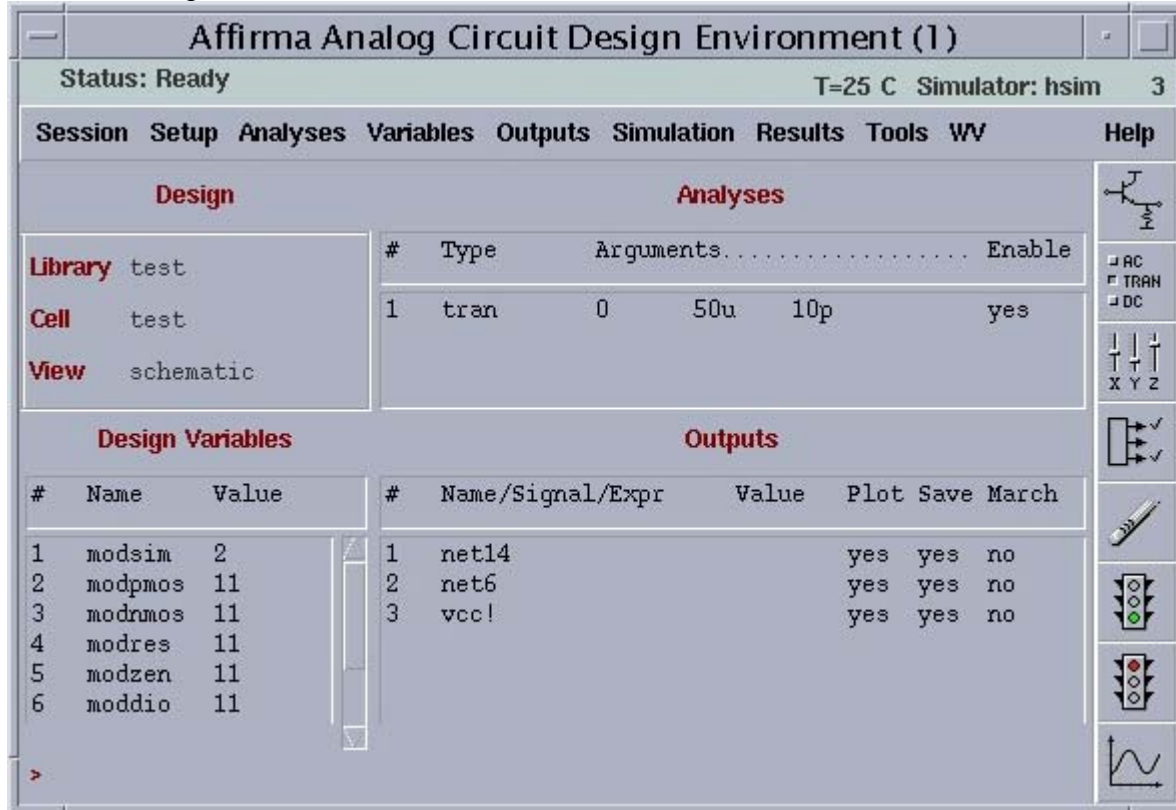
- 1.) Install HSIM analog Artist Interface code.
- 2.) Invoke icms
- 3.) Run the skill command `createHSIMView("libraryName")`
- 4.) Run the skill Command `createHSIMSimInfo("libraryName")`
- 5.) Check cdf simulation info for HSIM and updates.

This procedure will update the library. These commands have many options. One option is to convert only one cell. As with any conversion software, this code does most of the work, but you need to understand and apply it correctly. The HSIM User Manual has a lot of detail and the support from Nassda has been excellent. When the libraries are converted and the software installed the HSIM Artist Environment will have a similar look to spectreS and hspice. The HSIM simulator adds high speed circuit simulation (5-100X), power analysis, timing analysis, and multiple waveform viewer support (nWaves, WaveView, AWD and Signalscan) to the Analog Artist environment.

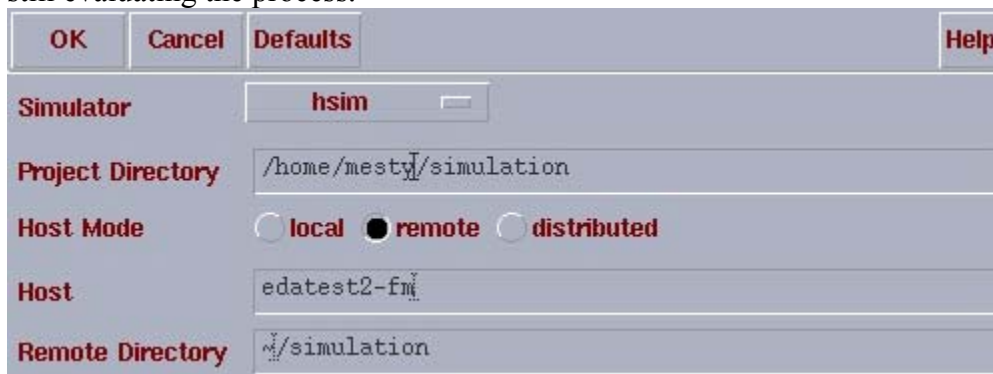
## **Analog Artist HSIM environment**

The following section is an overview of the current Analog Artist HSIM interface. This will demonstrate the interface and will not describe all the details.

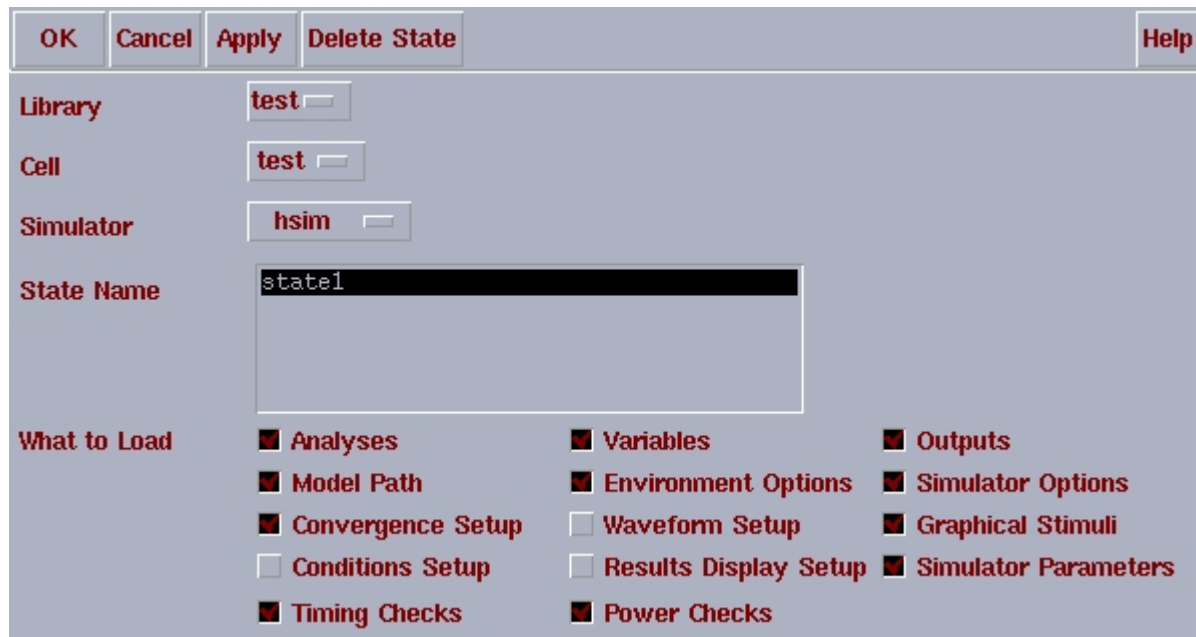
The Affirma Analog Artist Circuit Design Environment window look the same as other simulator setups. It indicates HSIM as the simulator and has a menu for Sandworks Waveview



This is the dialog box to select HSIM. In this example, I have selected a Linux workstation to run the simulation on. These ran faster and we have not had any issues with the simulations. We are still evaluating the process.



The standard statefile dialog box



A standard statefile dialog box with a light blue background. At the top are buttons for OK, Cancel, Apply, Delete State, and Help. The main area contains labels for Library, Cell, Simulator, and State Name, each followed by a text input field. The State Name field contains 'state1'. Below these is a 'What to Load' section with a grid of checkboxes for various simulation options.

Library	test															
Cell	test															
Simulator	hsim															
State Name	state1															
What to Load	<table><tr><td><input checked="" type="checkbox"/> Analyses</td><td><input checked="" type="checkbox"/> Variables</td><td><input checked="" type="checkbox"/> Outputs</td></tr><tr><td><input checked="" type="checkbox"/> Model Path</td><td><input checked="" type="checkbox"/> Environment Options</td><td><input checked="" type="checkbox"/> Simulator Options</td></tr><tr><td><input checked="" type="checkbox"/> Convergence Setup</td><td><input type="checkbox"/> Waveform Setup</td><td><input checked="" type="checkbox"/> Graphical Stimuli</td></tr><tr><td><input type="checkbox"/> Conditions Setup</td><td><input type="checkbox"/> Results Display Setup</td><td><input checked="" type="checkbox"/> Simulator Parameters</td></tr><tr><td><input checked="" type="checkbox"/> Timing Checks</td><td><input checked="" type="checkbox"/> Power Checks</td><td></td></tr></table>	<input checked="" type="checkbox"/> Analyses	<input checked="" type="checkbox"/> Variables	<input checked="" type="checkbox"/> Outputs	<input checked="" type="checkbox"/> Model Path	<input checked="" type="checkbox"/> Environment Options	<input checked="" type="checkbox"/> Simulator Options	<input checked="" type="checkbox"/> Convergence Setup	<input type="checkbox"/> Waveform Setup	<input checked="" type="checkbox"/> Graphical Stimuli	<input type="checkbox"/> Conditions Setup	<input type="checkbox"/> Results Display Setup	<input checked="" type="checkbox"/> Simulator Parameters	<input checked="" type="checkbox"/> Timing Checks	<input checked="" type="checkbox"/> Power Checks	
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<input type="checkbox"/> Conditions Setup	<input type="checkbox"/> Results Display Setup	<input checked="" type="checkbox"/> Simulator Parameters														
<input checked="" type="checkbox"/> Timing Checks	<input checked="" type="checkbox"/> Power Checks															

This dialog box is from the Simulation>HSIM Parameters selection.  
This is how to select different waveform databases to output.



A 'Basic HSIM Simulation Parameters' dialog box with a maroon title bar. It has buttons for OK, Cancel, Defaults, Apply, and Help. The main area contains several parameters with input fields or lists. The 'HSIMOUTPUT' field has a dropdown menu open showing options: psf, wdf, fsdb, nassda, and out. The 'HSIMPOSTL' field has radio buttons for 1, 2, and 3. The 'HSIMVDD' field is empty. The 'HSIMSPEED' field contains '3'. The 'HSIMANALOG' field contains '1'. The 'HSIMDCITER' field contains '250'.

Parameter	Value
HSIMOUTPUT	psf (dropdown menu open showing: psf, wdf, fsdb, nassda, out)
HSIMPOSTL	1 (radio buttons for 1, 2, 3)
HSIMVDD	
HSIMSPEED	3
HSIMANALOG	1
HSIMDCITER	250

## Timing Check Dialog Box

<b>OK</b>		<b>Cancel</b>		<b>Help</b>	
<b>Check List :</b>					
Title		Arguments			
<b>Add</b>		<b>Delete</b>		<b>Clear</b>	
<b>check type*</b>		setup time <input type="checkbox"/>			
<b>title*</b>		<input type="text"/>			
<b>setup time*</b>		<input type="text"/>			
<b>Signal :</b>			<b>Reference :</b>		
<b>name*</b>		<b>name*</b>			
<input type="text"/>		<input type="text"/>			
<input type="button" value="Select On Schematic"/>		<input type="button" value="Select On Schematic"/>			
<b>edge type:</b>		<b>edge type:</b>			
Rising <input type="checkbox"/>		Rising <input type="checkbox"/>			
<b>vlth</b>		<b>vlth</b>			
<input type="text"/>		<input type="text"/>			
<b>vhth</b>		<b>vhth</b>			
<input type="text"/>		<input type="text"/>			
<b>Subckt</b>		<input type="text"/>			
<b>Window</b>		<input type="text"/>			



Power Simulation Dialog Box

OK

Cancel

Help

Check List :

Title	Arguments
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Add

Delete

Clear

check type\*

dc path

title\*

node list\*

Select On Schematic

I\_threshold :

50u

period

start/stop

Start Time :

End Time :

1	<div></div>	<div></div>
2	<div></div>	<div></div>
3	<div></div>	<div></div>
4	<div></div>	<div></div>
5	<div></div>	<div></div>
6	<div></div>	<div></div>
7	<div></div>	<div></div>
8	<div></div>	<div></div>
9	<div></div>	<div></div>
10	<div></div>	<div></div>

Additional HSIM parameter dialog box.



The image shows a screenshot of the 'Advanced HSIM Simulation Parameters' dialog box. The title bar is dark blue with the text 'Advanced HSIM Simulation Parameters'. Below the title bar is a row of buttons: 'OK', 'Cancel', 'Defaults', 'Apply', and 'Help'. Below the buttons is a note: 'note: using spaces and quotes for list fields. Ex: "x1.x2.\*" "x1.\*.x2.\*" "/home/john/models.sp" "~/nodes/netlist"'. The main area of the dialog box is divided into two columns. The left column is labeled 'Control Parameters for:' and contains a list of parameters: 'HSIMGCAP', 'HSIMGCAPR', 'HSIMFCAP', 'HSIMFCAPR', and 'HSIMFCM'. The right column contains a list of simulation options: 'Ungrounded Capacitors', 'Grounded Capacitors', 'Isomorphic Matching', 'Flattening the Circuit Hierarchy', 'Simulation Time Scale', 'DC Initialization', 'Output Flush', 'Trapezoidal Integration Algorithm', 'General Simulation Control', 'Accuracy/Speed Trade-off', 'Device Model', 'MOSFET Table Model', 'bjt/diode Charge Conservation', 'Iteration', 'Node Capacitance Report', 'General Parser', 'Post-Layout Back-Annotation', 'Post-Layout RC Reduction', 'HSIM Output', and 'Digital Vector File'. A dropdown menu is open, showing the list of simulation options. The 'Ungrounded Capacitors' option is currently selected and highlighted in black.

Control Parameters for:	Simulation Options
HSIMGCAP	Ungrounded Capacitors
HSIMGCAPR	Grounded Capacitors
HSIMFCAP	Isomorphic Matching
HSIMFCAPR	Flattening the Circuit Hierarchy
HSIMFCM	Simulation Time Scale
	DC Initialization
	Output Flush
	Trapezoidal Integration Algorithm
	General Simulation Control
	Accuracy/Speed Trade-off
	Device Model
	MOSFET Table Model
	bjt/diode Charge Conservation
	Iteration
	Node Capacitance Report
	General Parser
	Post-Layout Back-Annotation
	Post-Layout RC Reduction
	HSIM Output
	Digital Vector File

## HSIM Waveform Viewers

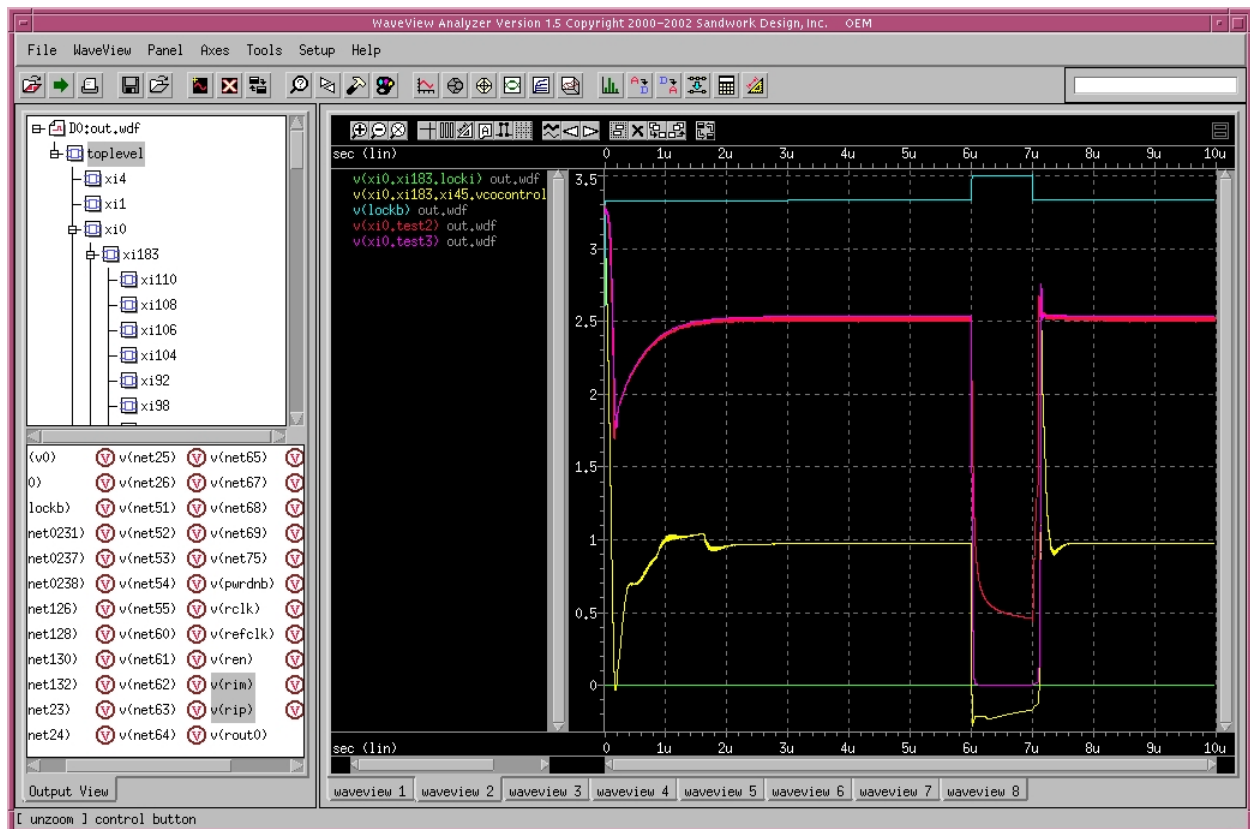
HSIM supports ASCII psf files and is currently improving the Analog Artist waveform viewer support. As described earlier, the Analog Artist waveform viewer, even with spectre, becomes unusable with a large simulation database. The Analog Artist Waveform viewer support of digital signals is limited. We had been using nWave as a waveform viewer. It is a fast viewer and works well. The Sandwork WaveView Analyzer has additional features:

- Integration into the Cadence environment
- Support of logic timing diagrams, analog plots, histograms, Smith charts, sweep plots, polar charts and eye diagrams.
- Fast waveform viewing

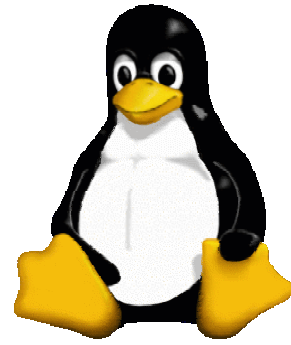
We have currently not completed our review of waveform viewers. Another option to review is SignalScan. The issue with SignalScan is that it is not well integrated into the Cadence Analog Artist Mixed-signal environment and to implement the entire Cadence AMS environment is a high price to pay for a fast waveform viewer.

## Sandwork WaveView Analyzer

This waveform viewer is an add on product that can be used with HSIM.



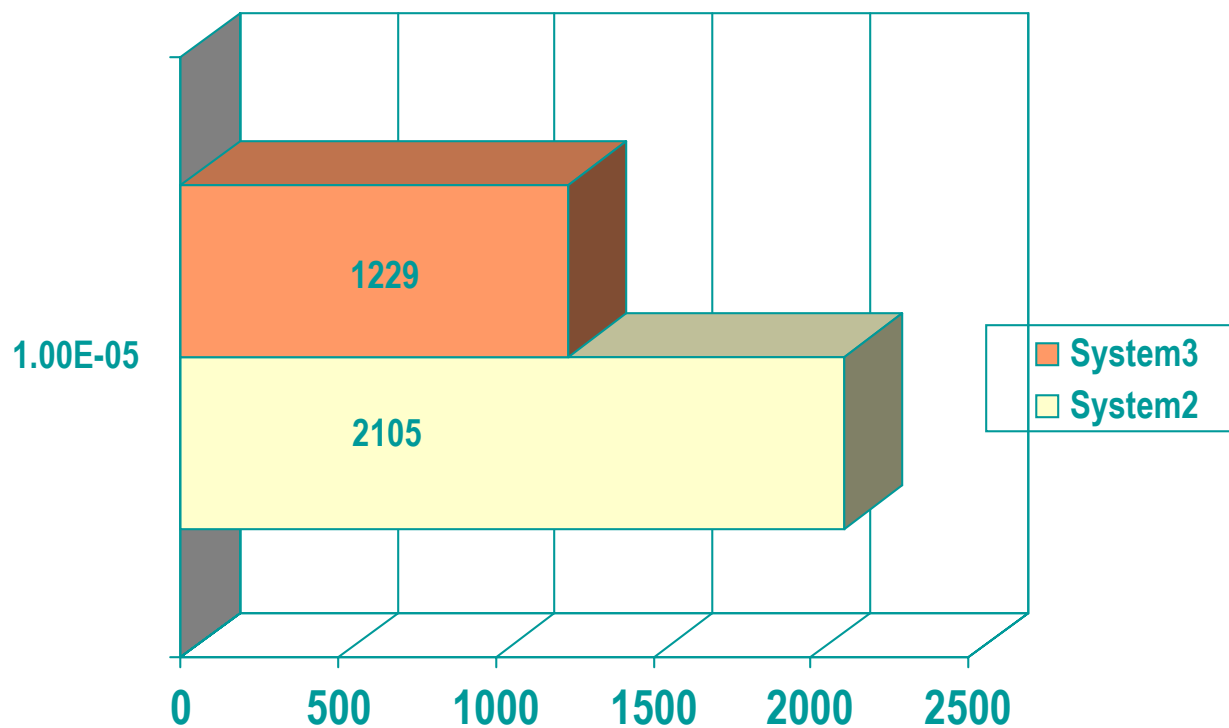
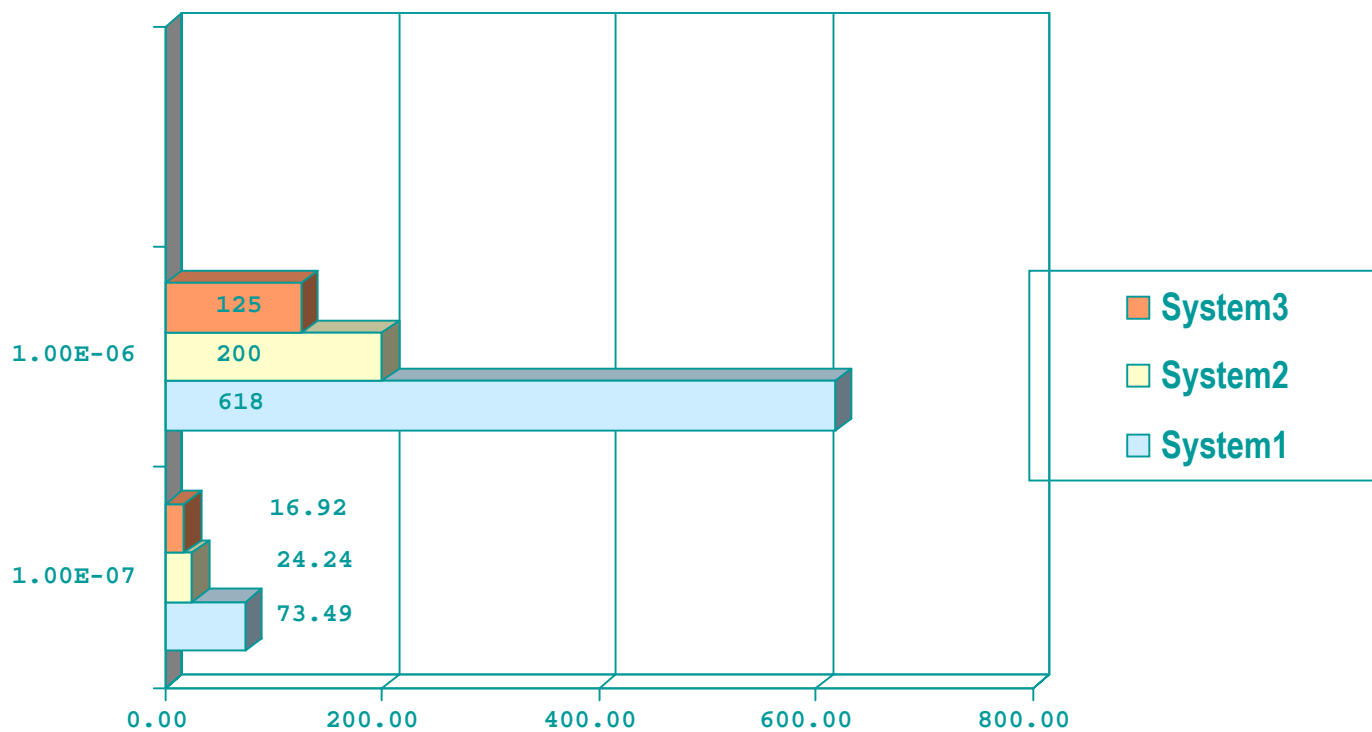
## HSIM on the the Linux operating system



We are currently evaluating setting up and running simulations on Linux platforms. Setting up Linux compute farms and running simulation corner sets in parallel can significantly reduce simulation time. There are many issues with benchmarks. We have found the data reflects real world usage. We have also seen other simulators speed increase similarly. I would encourage you to run your own test. Spice is very CPU intensive and performance is related to processor speed. We ran HSIM on several platforms. Here is the data from the HSIM runs.

### Test Equipment

- System 1 - Sun Ultra 5, Single 333 Mhz UltraSPARC Ili cpu, 256 Mbytes of ram, and 1 - 9 Gbyte IDE harddrive.
- System 2 - Sun SunBlade 1000, Dual 900 Mhz UltraSPARC III cpu's, 2048 Mbytes of ram, and 2 - 36 Gbyte SCSI fiberchannel harddrives
- System 3 - Dell Precision 340, Single 2.2 Ghz Pentium 4, 1024 Mbytes Ram, and 40 Gbyte IDE harddrive



## **Conclusion**

This paper is an overview of adding HSIM into a mixed-signal design process. This methodology has been applied to several designs that have taped out. This methodology can be applied to many designs. At Fairchild, the designers have adopted using HSIM for many types of simulations. It has improved the iteration time and accuracy at the beginning of the design cycle.

The application does not resolve all issues. It is not used for simulations that need higher accuracy than it provides. It does not run faster than Verilog. In the methodology described, it has proven to be very useful. The support of Linux adds additional speed. The support of different waveform viewers has improved the speed of analysis after simulations. We were looking a Nassda HSIM as a High Speed simulator for power, RC and timing analysis for large digital circuits. The methodology described in this paper is in addition to those benefits.